Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **A1**
2. **B1**
3. **N. CLR1**
4. **N. Q1**
5. **Q2**
6. **CEXT2**
7. **REXT/CEST**
8. **GND**
9. **A2**
10. **B2**
11. **N. CLR2**
12. **N. Q2**
13. **Q1**
14. **CEXT1**
15. **REXT/CEST**
16. **VCC**

**.052”**

**1 16**

**2**

**3**

**4**

**5**

**6**

**7**

**8 9**

**15**

**14**

**13**

**12**

**11**

**10**

**MASK**

**REF**

**5 1**

**4 2**

**H 3**

**C C**

**.081”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: 54HC123 C**

**APPROVED BY: DK DIE SIZE .052” X .081” DATE: 7/11/22**

**MFG: FAIRCHILD / NSC THICKNESS .015” P/N: 54HC123**

**DG 10.1.2**

#### Rev B, 7/19/02